UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/664,542	09/18/2000	Masahiro Tanaka	P108075-00017	4559

7590 04/13/2004

Arent Fox Kintner Plotkin & Kahn PLLC
1050 Connecticut Avenue NW
Suite 600
Washington, DC 20036-5339

EXAMINER	
AUVE, GLENN ALLEN	
ART UNIT	**PAPER NUMBER**
2111	9

DATE MAILED: 04/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/664,542	TANAKA, MASAHIRO	
	Examiner	Art Unit	
	Glenn A. Auve	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9 and 10* is/are allowed.

6)☒ Claim(s) *1-3,8 and 11-14* is/are rejected.

7)☒ Claim(s) *4-7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 September 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8*.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on January 28, 2004, has been entered.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 14 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 14 is rejected because it is not clear what is meant by "a data bus that generates control data" on lines 2-3. A bus is a passive element that does not have any sort of capacity to "generate" any sort of data. The bus can carry data, but some other element of logic like the CPU must generate the control data.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-3,8, and 12-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Japanese Patent Publication 63-313251 to Mitsubishi Electric Corp. (Mitsubishi) cited by applicant.

As per claim 1, Mitsubishi shows a first register (6) that stores data from the data bus (4) in response to an access signal supplied from the address bus (3); and a memory (2) that receives the data stored in the first register and inputs and outputs data from and to the data bus using the data as an address signal (throughout the abstract). Mitsubishi shows all of the elements recited in claim 1.

As for claim 2, the argument for claim 1 applies. Mitsubishi also shows an address generation circuit (8) that generates an address signal accessible by the memory and supplies the address signal to one of the memory and the first register. Mitsubishi shows all of the elements recited in claim 2.

As for claim 3, the argument for claim 2 applies. Mitsubishi also shows a second register (7) connected between the memory and the data bus for storing data from one of the data bus and the memory in response to the access signal. Mitsubishi shows all of the elements recited in claim 3.

As for claim 8, the argument for claim 1 applies. Mitsubishi also shows a decoder (8) connected to the address bus (3) to generate a control signal in response to the access signal; and a switch circuit connected between the memory and the data bus and being conductive in response to the control signal (also in decoder 8 which receives and processes access signals from bus 3 and outputs a control signal in response thereto to control the memory and the registers). Mitsubishi shows all of the elements recited in claim 8.

As per claim 12, Mitsubishi shows a data I/O system connected to an address bus and a data bus comprising: a first register (6) that stores data from the data bus (4) in response to an access signal supplied from the address bus (3); and a memory (2) that receives the data stored in the first register and inputs and outputs data from and to the data bus using the data as an address signal (throughout the abstract). Mitsubishi shows all of the elements recited in claim 12.

As per claim 13, Mitsubishi shows a CPU (1) connected to an address bus (3) and a data bus (4); a first register (6) that stores data from the data bus (4) in response to an access signal supplied from the address bus (3); and a memory (2) that receives the data stored in the first register and inputs and outputs data from and to the data bus using the data as an address signal (throughout the abstract). Mitsubishi shows all of the elements recited in claim 13.

Even though claim 14 has been rejected under 35 USC § 112, 2nd as being indefinite it is still being rejected based on the prior art. The claim is being interpreted such that the CPU generates control data. As per claim 14, Mitsubishi shows a CPU (1) connected to an address bus (3) and a data bus (4) that generates control data; an address generation circuit (8) that generates a sequence of addresses in response to the control data from the CPU; and a memory control circuit that accesses the memory in accordance with the sequence of addresses from the address generation circuit, wherein the control data indicates start and stop of the address generation circuit (abstract, wherein the registers 6 and 7 are written with address data obtained from the bus 4 in response to control signals received from the decoder circuit 8). Mitsubishi shows all of the elements recited in claim 14.

6. Claim 11 is rejected under 35 U.S.C. 102(b) as being anticipated by European Patent Application 0 554 819 A1 to Matsushita Electric Industrial Co., Ltd. (Matsushita) cited by applicant.

As per claim 11, Matsushita shows storing an address signal from an address bus in a register; writing data to a storage device in accordance with the address in the register; storing a circulating address signal in the register; and reading data from the storage device in accordance with the circulating address signal stored in the register (throughout col.2, line 34 – col.3, line 39). Matsushita shows all of the steps recited in claim 11.

Conclusion

7. Claims 4-7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. An English language translation is not readily available of the Japanese reference relied upon to reject the claims above. The document has been sent out for translation.

8. The following is a statement of reasons for the indication of allowable subject matter: At this point the prior art does not show the A/D and D/A conversion operations recited in claims 9 and 10, however it is possible that the translated prior art documents may show these limitations, and the examiner reserves the option to reject these claims in a future action depending on what the prior art ultimately shows.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Glenn A. Auve whose telephone number is (703) 305-9638. The examiner can normally be reached on M-Th 8:00 AM-5:30 PM, every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (703) 305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Glenn A. Auve
Primary Examiner
Art Unit 2111

gaa
April 12, 2004